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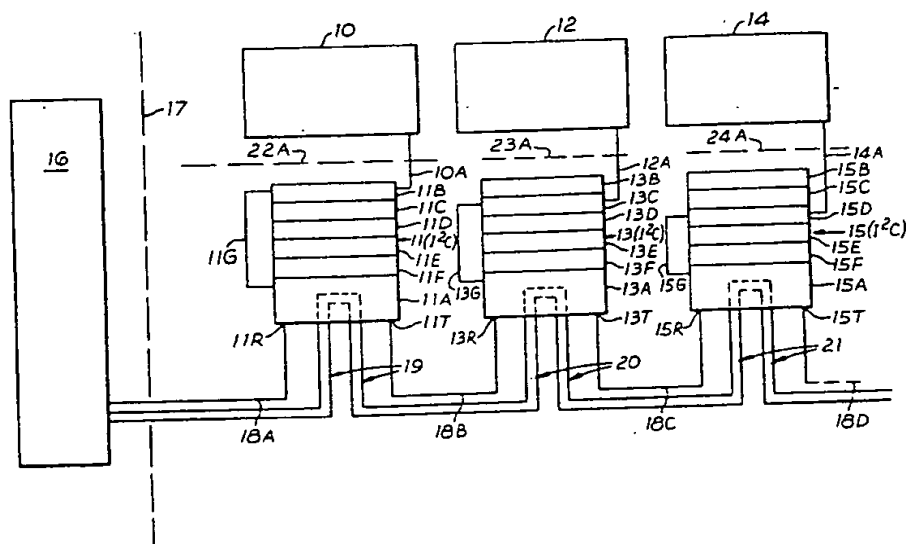
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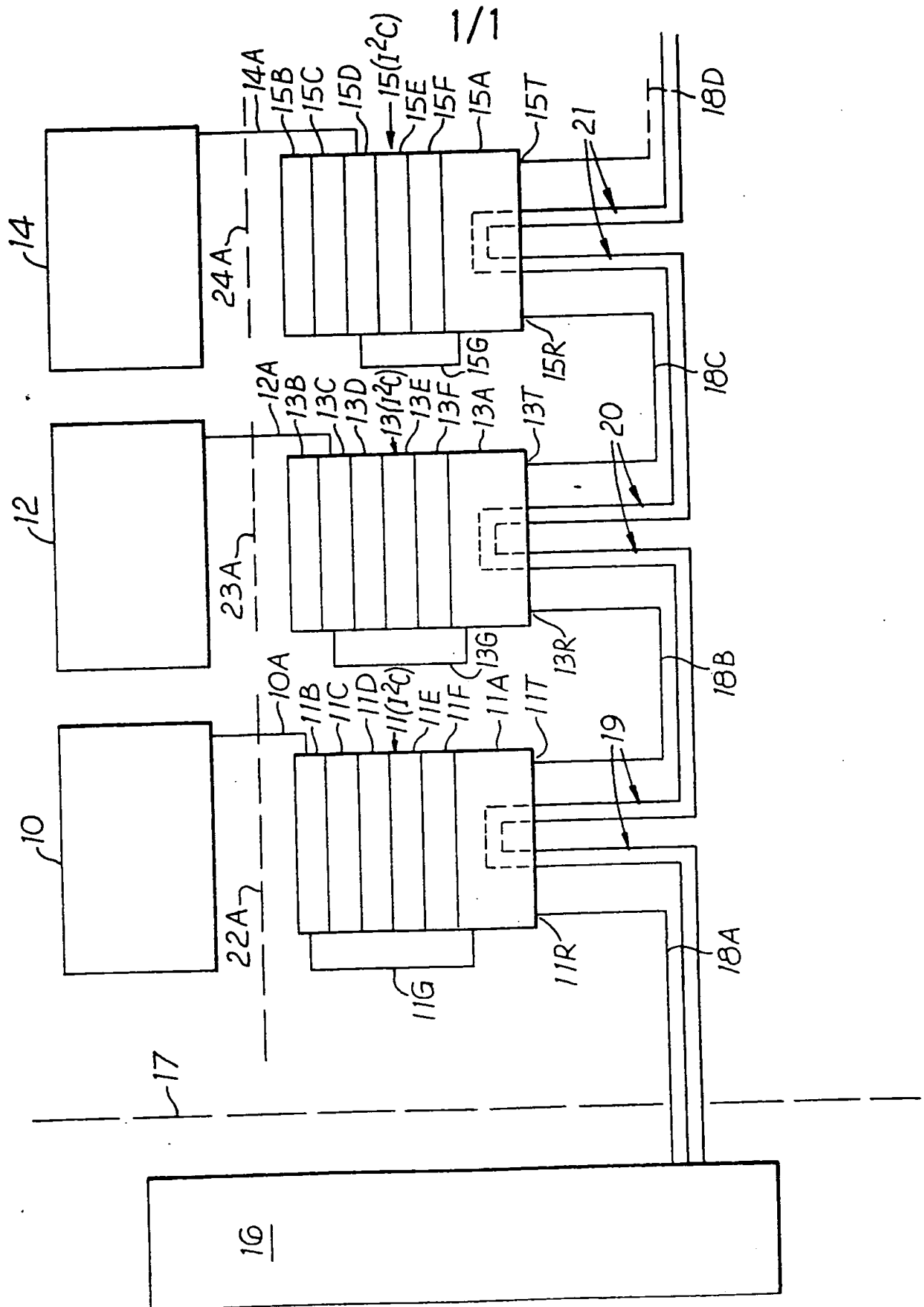
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## (54) Multi-processor system configuration

(57) Apparatus embodying a plurality of operational means 10, 12, 14 for performing respective functions is controlled by a control system including working units 11, 13, 15 in the form of microcontrollers having serial bus interfaces, at least some of the working units including means 11A, 13A, 15A settable by an address allocating signal derived from a main control processing unit 16 to any one of a plurality of addresses after initialisation of the working units in sequence by signals transmitted along a single serial channel 18A, 18B, 18C and including also selectable function means 11B-F, 13B-F, 15B-F. The operational means 10, 12, 14 receive signals from the selected function means and/or from the main central processing unit 16.





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## APPARATUS FOR SETTING PROCESSOR ADDRESSES

This invention relates to an apparatus (herein called the main apparatus) comprising a plurality of operational means each required to perform a respective function (which may be different in respect of each of  
5 the operational means or common to some or all of them) beginning at co-ordinated starting times and for this purpose controlled by a control system. The latter comprising at least one central (computer) processing unit (herein called the main CPU), and a plurality of  
10 slave (computer) processing units (herein called working units), associated respectively with the operational means, and communication means establishing communication between the main CPU and the working units to enable the latter to receive and transmit signals appropriate to  
15 their functions for bringing about operation of their respectively associated operational means. Such apparatus is herein called apparatus of the kind specified.

One of the objects of the present invention is to  
20 provide, in an apparatus of the kind specified, a control system which is capable of meeting the requirements of a number of different forms of main apparatus especially in respect of the numbers of operational means embodied therein and in respect of different types of operational  
25 means.

According to the present invention there is provided an apparatus of the kind specified wherein at least one of the working units includes a first means, herein called the address means, settable by an

appropriate address signal to establish any one of a plurality of different addresses for the working unit, and a plurality of second means, herein called the function means, able to establish respective output  
5 signals appropriate to respective ones of the operational means of the apparatus, means for selecting which of the function means is to be controlled by the address means capable of being rendered operative during working of the apparatus, and wherein the main CPU provides for the  
10 transmission of appropriate signals to set the address of each of the address means of the working units, and subsequently to address the or each working unit to bring the selected function means and hence the respectively associated operational means into operation.

15 According to a further feature at least a plurality of the working units may each include an initialising means having an input terminal requiring a first predetermined signal state to be established thereon to initialise the working unit and an output terminal on  
20 which a corresponding state is also established at the end of an initialising routine performed by the unit after establishment of said first state means, the working units being arranged to be initialised in sequence by a channel (herein called the serial chain  
25 channel) provided by the communication means effectively establishing a chain of communication starting from the main CPU to the input terminal of a first one of the working units and continuing to the input terminal of each successive working unit from the output terminal of  
30 the preceding one of the working units.

The term "initialising" and its derivatives is used herein in the manner conventionally understood in the art to mean conversion of the working unit concerned from a

state in which entities therein during operation are required to attain given (but possibly varying) electrical potentials to an initial state in which they have respective predetermined starting potentials. In particular but not exclusively one form of initialising routine is one in which an address means included in the working unit is brought into a condition in which it is able to be set to respond to a predetermined address code transmitted to it from the main CPU and will respond exclusively to that code.

The invention will now be described with reference to the accompanying diagrammatic drawing which shows schematically an apparatus of the kind specified embodying three operational means of the main apparatus respectively associated working units and a main CPU.

The apparatus may be in the form of a vending machine and whilst a wide variety of operational units may be incorporated it is mentioned by way of example that the first operational unit 10 may be a card reader for reading a card, herein called a club card, inserted into, or swiped through a suitable slot in the machine by a user and embodying a record member. The card may carry a record of the identity of the user and of various data items applicable to the type of main apparatus, goods vended, class of user, site of apparatus and other matters. It could be programmed to record a credit of a given amount applicable to that user and that card, it being assumed that the user will have prepaid the amount in question to some suitable receiving station. The purpose of the operational means 10 is to render the machine usable by the particular user inserting the card. As a possible alternative the operational means 10 may comprise a coin-receiving device which, in response to

insertion of a coin or coins of the appropriate denomination or denominations renders the machine usable. In yet another alternative arrangement the operational means 10 may be a printer and for convenience in the following description it will be assumed to be such.

The operational means 12 may comprise a credit register for reading the credit still available to the user and possibly provided with means for decrementing this credit as a function of the number of vends for which a particular club card has been used by insertion into the operational means 10.

The operational means 14 may comprise a means for rendering articles for vending or renting available to the user either by unlocking a locked compartment containing the article or moving the compartment between a position in which the article is accessible and can be taken out by the user or replaced when necessary and a position in which the article is not so accessible.

It will be understood that other operational means may be provided which have been omitted for simplicity, for example means indicating what articles are present or the number of any given articles present, and means indicating whether the user has correctly operated the machine and possibly displaying instructions to facilitate correct operation.

Associated operatively with each of the operating means 10, 12 and 14 is a working unit, these being designated 11, 13 and 15. Each may comprise a microcontroller with a serial bus interface and which may be of the type designated Mullard I<sup>2</sup> C. Referring to the working unit 11 (I<sup>2</sup> C) this integrated circuit unit

includes an address means 11A settable by an appropriate address allocating input signal to establish any one of a plurality of addresses for the working unit 11. The unit further includes a plurality of functional means 11A, 11B, 11C, 11E, 11F, which can be hard wired on the board containing the  $I^2C$  integrated circuit unit each to perform certain of the functions required to bring about operation of the means 10, 12, 14. In each working unit only one of the functional means 11B to 11F will be so wired and that one will be connected appropriately (e.g. by hard wiring) to the address means 11A, or 13A, or 15A as the case may be to be brought into operation when the address means is correctly addressed. Thus the  $I^2C$  units incorporated in the working unit or boards 11, 13, 15 can be of common form (identical) leading to considerable economy in their provision.

Corresponding address means 13A, 15A and functional means 13B-13F and 15B-15F are provided respectively in the working units 13 ( $I^2C$ ) and 15 ( $I^2C$ ) except that (as mentioned) the functional means able to be brought into use on the units 13 ( $I^2C$ ) and 15 ( $I^2C$ ) and selected by appropriate wiring are different in these units as required by the different characters of the operational means 12 and 14. Not all of the functions to be performed by the operating units 10, 12, 14 will normally be brought about or controlled solely by the selected functional units 11B, 13C and 15D as indicated schematically by the hard wiring links 10A, 12A, 14A established through interface means 22A, 23A, 24A and by the controlling hard wiring links 11G, 13G, 15G from the address means 11A, 15A to the selected functional means 11B, 13C, 15D. Signals from supplementary functional means included in the main CPU will usually be required to achieve full performance of the intended functions of

the operating means. For example when the operating means 10 is a printer the working unit 11B may contain the paging, line spacing, word spacing and similar "housekeeping" functions but the signals providing the text or graphics will usually be derived from a supplementary functional means in the main CPU. Once the main CPU has correctly addressed the unit 11 this will serve not only to access the supplementary signals to the functional means 11A and operating means 10 but because the supplementary functional means in the main CPU is uniquely functionally associated with the means in the CPU providing the correct address signal this will ensure that these supplementary signals are supplied to and effective in only the unit 11.

The working units are controlled as to their time of operation by a main CPU 16. The address and functional signals from the main CPU are conveyed through bus means 18 which is shown in double lines to signify that it contains a plurality of separate conductors. In the present case there may be five conductors one of which, acting as a serial chain channel, is for convenience shown separately at 18A, 18B, 18C and 18D. The remaining conductors of the bus means are shown as having links 19, 20, 21 interfacing with respective address means and functional means of the working units and may be allocated to the functions respectively of data, clock signal, 0-volt (common), and 24-volt transmission.

There will now be described how a working unit is initialised and thereby placed in a condition to receive and transmit an address signal along the conductor 18A forming the first part of the serial chain channel of the bus means 18. All of the units are held initially in a

"reset" state "0" and are sequentially released one at a time. This is achieved by removing the reset signal from the input terminal which is the reset terminal of the working unit (designated 11R for the unit 11). Until the  
 5 reset signal has been removed from the input terminal the working unit is incapable of subsequently receiving or transmitting any instructions.

When the reset signal has been removed from terminal 11R of the first working unit this unit starts  
 10 an initialising routine by means incorporated in it for this purpose and it is then in a state to transmit and receive information, address codes, and other data to and from the main CPU 16. All other working units are not so capable until they have been initialised and performed  
 15 their respective initialising routines.

The establishment of an address in the address means 11A, 13A, 15A, of each  $I^2C$  unit can be brought about in alternative ways.

In the first (simpler) way the main CPU 16 includes  
 20 means for storing in effect a table comprising address codes and functional signals. Thus a plurality of (different) address codes will each pertain to a particular form of operating means e.g. printer, display means, etc. The correlation i.e. association between a  
 25 particular address code and a particular form of operating means may be established by ensuring that each address code is followed (when the apparatus is in full operation) uniquely by signals providing the functions supplementing those brought about by the functional means  
 30 of the working unit appropriate to the associated operating means e.g., an address code furnished by the main CPU for a working unit controlling a printer would

be correlated, i.e. followed, by signals bringing about printing of textual information, (the function means 11B for example providing the paging etc function).

Thus in address allocation by this first mode,  
5 initialisation of unit 11 would be followed by transmission to it of the address code pre-stored in the main CPU 16 and which is correlated with the supplementary functional data appropriate to a printing means.

10 The store means for the pre-stored address codes of the main CPU would be assigned to output (i.e. furnish) these in the sequence of initialising the units 11, 13, 15 etc. This requires that the units 11, 13, 15 have to be connected in the bus conductor 18A, 18B, 18C in the  
15 proper (physical) sequence. This may not always be convenient and the second way of establishing addresses is more flexible.

In this second embodiment of the invention, although the various operating means still require to be  
20 brought into operation in a predetermined order, the various I<sup>2</sup>C working units 11, 13, 15 controlling them can be connected in the bus in any order.

The main CPU 16 has (as before) means for storing a plurality of (different) address codes respectively  
25 associated with means for furnishing (from store means) supplementary function signals appropriate to respective (companion) functional means e.g. 11B, 13C, 15D.

After initialisation of any working unit, say 11, it is arranged to transmit to the main CPU an  
30 identification signal which identifies the functional

means e.g. 11B which has been selected (by the hard wiring configuration) as appropriate to control the operating means 10 e.g. a printer. The main CPU 16 includes means for recognising the identification signal and, in response to receipt of the identification signal, thereafter transmitting to the address means of the working unit 11 that address code which is associated with the proper supplementary signal store e.g. one furnishing supplementary printing signals.

Thus in operation as each working unit is initiated its address means can have set into it the proper address appropriate to its selected functional means irrespective of the (physical) position of its connection in the bus means.

Reverting to the initialisation routine, at the end of the initialising routine performed by unit 11 (after allocation and transmission of its address code from the main CPU 16) the output terminal 11T is caused to remove the reset signal via channel 18B from the input terminal 13R of the next succeeding working unit 13. At this stage unit 11 will have been given its operative address and consequently only unit 13 will perform an initialising routine and will then receive from the main CPU its operative address code, or transmit a function identity signal to, and thereafter receive (its own distinctive) operative address code from, the main CPU 16.

Subsequent, sequential initialising of the working unit 15 initiated from output terminal 13T of unit 13 occurs in a like manner.

Thus address codes can be simply and easily allocated to the working units without utilisation of

more than one channel in the communication means thus greatly simplifying the hardware of the main CPU and working units and the software for any given form of main apparatus and mode of operation.

5           Although the communication means to establish initialisation of the I<sup>2</sup>C units 11, 13 and 15 in sequence preferably utilises only a single channel in the form of a conductor i.e. comprising the wires 18A, 18B, 18C it would be possible for the communication means to  
10           comprise a radio link in which similarly only a single channel need be used. Further, it is within the scope of the invention for the bus means to be in the form of a ring from which sub-links such as 19, 20, 21 interface with respective working units instead of an open-ended  
15           chain as illustrated. This however would not apply to the serial chain channel 18A, 18B, 18C.

          It will be apparent that each working unit such as 11 and its associated operational means 10 can be brought into operation in sequence although the operations of  
20           these units may overlap in real time.

          Communication may be bi-directional along the bus means 18 from each of the working units which can signal its state and enable the main CPU to recognise and if need be monitor and signal the function performed by the  
25           associated operational means 10, 12 and 14 as the case may be.

          The control system is thus extremely flexible in the sense that it can be readily adapted economically to meet the requirements of a wide variety of different  
30           forms of main apparatus.

Further the employment of a single conductor 18A, 18B, 18C incorporated in the bus means to provide a serial communication channel for initialising each working unit in sequence permits other conductors in the bus means and other terminals on each working unit to be  
5 utilised for other purposes, that is feeding input and output signals to the main CPU or to the associated operational means 10, 12 and 14 as the case may be.

## CLAIMS

1. An apparatus of the kind specified wherein at least one of the working units includes a first means, herein called the address means, settable by an appropriate address signal to establish any one of a plurality of  
5 different addresses for the working unit, and a plurality of second means, herein called the function means, able to establish respective output signals appropriate to respective ones of the operational means of the apparatus, means for selecting which of the function  
10 means is to be controlled by the address means and capable of being operative during working of the apparatus, and wherein the main CPU provides for the transmission of appropriate signals to set the address of each of the address means of the working units; and  
15 subsequently to address the or each working unit to bring the selected function means and hence the respectively associated operational means into operation.

2. Apparatus according to Claim 1 wherein the main CPU includes means for storing a plurality of the address  
20 signals for setting different addresses into the address means of the working units, means for storing a plurality of function signals, herein called supplementary function signals, appropriate respectively to initiate and/or supplement the output signals of respective ones of the  
25 function means of the working units (herein called the companion function means) and correlated in a pre-ordained manner with respective ones of the stored address signals to enable the latter to be outputted to those respective working units in which the companion  
30 function means have been selected.

3. Apparatus according to Claim 1 wherein the main CPU includes means for storing a plurality of function signals appropriate respectively to initiate and/or supplement the output signals of respective ones of the function means (herein called the companion function means), means for recognising input signals (herein called the identity signals) received from respective ones of the working units and identifying the selected functional means of the working unit concerned, means for generating and storing a plurality of different address signals, means for outputting respective ones of these address signals to the working units respectively in response to receipt of an identifying signal therefrom and means for allocating each outputted address signal to a respective one of the supplementary function signals such that upon subsequent outputting of any address signal from the main CPU it is followed by the supplementary functional signal appropriate to the companion functional means of the working unit of which the address means has been set to that address.

4. Apparatus according to any of Claims 1 to 3 wherein at least a plurality of the working units each includes an input terminal requiring a first predetermined signal state to be established thereon to initialise the working unit and an output terminal on which a corresponding state is also established at the end of an initialising routine performed by the unit after establishment of said first state, the working units being arranged to be initialised in sequence by a channel (herein called the serial chain channel) provided by the communication means effectively establishing a chain of communication starting from the main CPU to the input terminal of a first one of the working units and continuing to the

input terminal of each successive working unit from the output terminal of the preceding one of the working units.

5        5.        Apparatus according to Claim 4 wherein transmission of the function identity signal and address code is arranged to be effected by way of the serial chain channel.

10       6.        Apparatus according to any one of Claims 2 to 4 wherein the input terminal is the reset terminal of the working unit concerned.

7.        Apparatus according to any one of the preceding claims wherein each of the plurality of working units comprises a microcontroller with an inter-integrated serial bus face.

15       8.        Apparatus substantially as hereinbefore described with reference to the accompanying drawing.

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